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;*******************************************************************************
;* MULTIPLE FORMAT VIDEO AGC/SYNC LOOP REGULATOR                               *
;* Written by: J.L.K. Electronics                                              *
;* Date: November 1, 2008                                                      *
;* Version: L                                                                  *
;* Format: NTSC/PAL/SECAM                                                      *
;* Mode: Basic VBI Regulation of All Formats/Format Auto Detect                *
;* MCU: ATtiny2313/V                                                           *
;* Clock Frequency: 20 MHz                                                     *
;* Reference Generator: LM1881                                                 *
;*******************************************************************************

; Program regulates the sync signal during the Vertical Blanking Interval (VBI) of
; NTSC, PAL and SECAM formats in the most basic form with the enhancement of format
; auto detect over Version J.  The detection of the vertical sync pulse generates
; an interrupt in the main loop program as in version J.  The program also directs
; the microcontroller (MCU) to pass the remaining vertical pulses unaltered as in
; Version J.  During the passing of these remaining pulses, a predetermined time
; is allowed to pass.  The end of this time corresponds to the difference between
; the duration of four vertical sync pulses of the NTSC format and four vertical
; sync pulses of the PAL/SECAM formats.  A test of the state of the composite sync
; signal at the pre-determined time identifies the format being processed.  The
; progam is then directed to the proper subroutine of the detected format and the
; composite sync signal is processed in the same manner as described in Version J.

;*******************************************************************************

.include "Tn2313def.inc"

; Interrupt service vectors

.org $0000
      rjmp  RESET                   ; Reset vector
.org INT1addr
      rjmp  INTV1                   ; Int1 vector (external interrupt from pin PD3)

;*******************************************************************************
;
; Declarations

.def temp   =r16                    ; Output to Port B in binary
.def temp1  =r17                    ; Pulse count in decimal
.def temp2  =r18                    ; Time cycles in hex
.def temp3  =r19                    ; Time cycle overflow in decimal

;*******************************************************************************
;
; Reset vector just sets up interrupts and service routine and then loops forever

RESET:
      ldi   temp,LOW(RAMEND)        ; Stack pointer
      out   SPL,temp                ;

      ldi   temp,0b11111111         ; Port B - Outputs
      out   DDRB,temp               ;
      ldi   temp,0b00000000         ; Port D - Inputs
      out   DDRD,temp               ;

      ldi   temp,0b00110100         ; Let all signals pass unaltered
      out   PORTB,temp              ;
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      ldi   temp,0b11111111        ; Pull-ups on all inputs
      out   PORTD,temp             ;

; Set up interrupt INT1

      ldi   temp,0b10000000        ; Int1 selected
      out   GIMSK,temp             ;
      ldi   temp,0b00001000        ; Falling edge of Int1
      out   MCUCR,temp             ;

      sei                          ; Set global interrupt flag

LOOP:
      rjmp  LOOP                   ;

;*****************************************************************************
;
; INT1 vector - passes vertical pulses unaltered - detects current format
;             - directs program to proper subroutine

INTV1:
      sbic  $10,4                  ; Test for first serration completion
      rjmp  INTV1                  ; Return to test
      ldi   temp3,4                ; Load vertical serration/pulse time overflow
V1:
      ldi   temp2,$D3              ; Load 31.65us ($D3=211;  211 x 0.15 = 31.65)
V2:
      dec   temp2                  ; Time adds to 127.3us at end of V2
      brne  V2                     ; NTSC is 127.1us and PAL/SECAM is 128us
      dec   temp3                  ;
      brne  V1                     ;
V3:
      ldi   temp2,$01              ; Time trimmer of 0.15us
V4:
      dec   temp2                  ;
      brne  V4                     ;
      sbic  $10,4                  ; Time at end of sbic if clear is 127.55us
      rjmp  PAL                    ; Jump to PAL/SECAM                    ;
      ldi   temp2,$C0              ; Load 28.8us ($C0=192; 192 x 0.15 = 28.8)
V5:
      dec   temp2                  ;
      brne  V5                     ;
      ldi   temp1,6                ;
V6:
      sbic  $10,4                  ; Test for post-equalizing pulse
      rjmp  V6                     ; Return to test
      ldi   temp,0b00100000        ; Load post-equalizing pulse
      out   PORTB,temp             ; Output post-equalizing pulse
      ldi   temp2,$0B              ; Load 1.65us ($0B=11; 11 x 0.15 = 1.65)
V7:
      dec   temp2                  ; Plus 13 clock cycles equals 0.65us
      brne  V7                     ; Subtotal equals 2.3us
      dec   temp1                  ;
      breq  V9                     ;
      nop                          ;
      nop                          ;
      nop                          ;
      nop                          ;
      nop                          ;
      ldi   temp,0b00001100        ; Load P-P interval
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        out     PORTB,temp              ; Output P-P interval
        ldi     temp2,$C2               ; Load 29.1us ($C2=194; 194 x 0.15 = 29.1)
V8:
        dec     temp2                   ; Plus 4 clock cycles equals 0.2us
        brne    V8                      ; Subtotal equals 29.3us
        ldi     temp,0b00110100         ; Load pass signal unaltered
        out     PORTB,temp              ; Output pass signal unaltered
        rjmp    V6                      ; Return to test
V9:
        sbic    $10,5                   ; Field detect
        rjmp    ODD                     ; Go to Odd field subroutine
        rjmp    EVEN                    ; Go to EVEN field detect

;*****************************************************************************
;
; Odd field subroutine for NTSC SDTV video signal input

ODD:
        nop                             ;
        ldi     temp,0b00001100         ; Load odd field P-P half-line
        out     PORTB,temp              ; Output odd field P-P half-line
        ldi     temp2,$C1               ; Load 28.95us ($C1=193; 193 x 0.15 = 28.95)
O1:
        dec     temp2                   ; Plus 3 clock cycles equals 0.15us
        brne    O1                      ; 2.3 + 28.95 = 0.15 = 31.4us
        ldi     temp1,11                ; Load VBI line 10 thru 20, inclusive
O2:
        ldi     temp,0b00110100         ; Load pass signal unaltered
        out     PORTB,temp              ; Output pass signal unaltered
O3:
        sbic    $10,4                   ; Test for horizontal sync pulse
        rjmp    O3                      ; Return to test
        ldi     temp,0b00100000         ; Load horizontal sync pulse
        out     PORTB,temp              ; Output horizontal sync pulse
        ldi     temp2,$1D               ; Load 4.335us ($1D=29; 29 x 0.15 = 4.35)
O4:
        dec     temp2                   ; Plus 7 clock cycles equals 0.35us
        brne    O4                      ; Subtotal equals 4.7us
        nop                             ;
        ldi     temp,0b00011100         ; Load breezeway and colorburst
        out     PORTB,temp              ; Output breezeway and colorburst
        ldi     temp2,$16               ; Load 3.3us ($16=22; 22 x 0.15 = 3.3)
O5:
        dec     temp2                   ; Plus 2 clock cycles equals 0.1us
        brne    O5                      ; Subtotal equals 3.4us
        ldi     temp,0b00001100         ; Load back porch remainder and P-P full line
        out     PORTB,temp              ; Output back porch remainder and P-P full line
        ldi     temp2,$D6               ; Load 53.5us ($D6=214; 214 x 0.25 = 53.5)
O6:
        nop                             ; Plus 5 clock cycles equals 0.25us
        nop                             ; Subtotal equals 53.75us
        dec     temp2                   ; Line total equals 61.85us
        brne    O6                      ; 1.5us front porch not included
        dec     temp1                   ; Countdown VBI lines
        brne    O2                      ; Finish VBI lines
        nop                             ;
        ldi     temp,0b00110100         ; Load pass signal unaltered
        out     PORTB,temp              ; Output pass signal unaltered
        reti                            ; Wait for next vertical pulse
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;*******************************************************************************
;
; Even field subroutine for NTSC SDTV video signal input

EVEN:
      ldi   temp1,11                ; Load VBI lines 273 thru 283, inclusive
      nop                           ;
      nop                           ;
      ldi   temp2,$0F               ; Load 2.25us ($0F=15; 15 x 0.15 = 2.25)
E1:
      dec   temp2                   ; Plus 16 clock cycles equals 0.8us
      brne  E1                      ; 1.65 + 0.8 + 2.25 = 4.7us
      ldi   temp,0b00011100         ; Load breezeway and colorburst
      out   PORTB,temp              ; Output breezeway and colorburst
      ldi   temp2,$16               ; Load 3.3us ($16=22; 22 x 0.15 = 3.3)
E2:
      dec   temp2                   ; Plus 2 clock cycles equals 0.1us
      brne  E2                      ; Subtotal equals 3.4us
      ldi   temp,0b00001100         ; Load back porch remainder and P-P full line
      out   PORTB,temp              ; Output back porch remainder and P-P full line
      ldi   temp2,$D6               ; Load 53.5us ($D6=214; 214 x 0.25 = 53.5)
E3:
      nop                           ; Plus 5 clock cycles equals 0.25us
      nop                           ; Subtotal equals 53.75us
      dec   temp2                   ; Line total equals 61.85us
      brne  E3                      ;
      nop                           ;
      nop                           ;
      nop                           ;
E4:
      ldi   temp,0b00110100         ; Load pass signal unaltered
      out   PORTB,temp              ; Output pass signal unaltered
E5:
      sbic  $10,4                   ; Test for horizontal sync pulse
      rjmp  E5                      ; Return to test
      ldi   temp,0b00100000         ; Load horizontal sync pulse
      out   PORTB,temp              ; Output horizontal sync pulse
      ldi   temp2,$1D               ; Load 4.35us ($1D=29; 29 x 0.15 = 4.35)
E6:
      dec   temp2                   ; Plus 7 clock cycles equals 0.35us
      brne  E6                      ; Subtotal equals 4.7us
      nop                           ;
      ldi   temp,0b00011100         ; Load breezeway and colorburst
      out   PORTB,temp              ; Output breezeway and colorburst
      ldi   temp2,$16               ; Load 3.3us ($16=22; 22 x 0.15 = 3.3)
E7:
      dec   temp2                   ; Plus 2 clock cycles equals 0.1us
      brne  E7                      ; Subtotal equals 3.4us
      ldi   temp,0b00001100         ; Load back porch remainder and P-P full line
      out   PORTB,temp              ; Output back porch remainder and P-P full line
      ldi   temp2,$D6               ; Load 53.5us ($D6=214; 214 x 0.25 = 53.5)
E8:
      nop                           ; Plus 5 clock cycles equals 0.25us
      nop                           ; Subtotal equals 53.75us
      dec   temp2                   ; Line total equals 61.85us
      brne  E8                      ; 1.5us front porch not included
      dec   temp1                   ; Countdown VBI lines
      brne  E4                      ; Finish VBI lines
      nop                           ;
      ldi   temp,0b00110100         ; Load pass signal unaltered
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      out   PORTB,temp              ; Output pass signal unaltered
      reti                          ; Wait for next vertical pulse

;*******************************************************************************
;
; PAL/SECAM VBI subroutine - generates post-equalizing pulses
;                          - determines field subroutine

PAL:
      ldi   temp1,5                 ; Load five post-equalizing pulses
PV1:
      sbic  $10,4                   ; Test for post-equalizing pulse
      rjmp  PAL                     ; Return to test
      ldi   temp,0b00100000         ; Load post-equalizing pulse
      out   PORTB,temp              ; Output post-equalizing pulse
      ldi   temp2,$0B               ; Load 1.65us ($0B=11; 11 x 0.15 = 1.65)
PV2:
      dec   temp2                   ; Plus 14 clock cycles equals 0.7us
      brne  PV2                     ; Subtotal equals 2.35us
      dec   temp1                   ;
      breq  PV4                     ;
      nop                           ;
      nop                           ;
      nop                           ;
      nop                           ;
      nop                           ;
      nop                           ;
      ldi   temp,0b00001100         ; Load P-P interval
      out   PORTB,temp              ; Output P-P interval
      ldi   temp2,$C3               ; Load 29.25us ($C3=195; 195 x 0.15 = 29.25)
PV3:
      dec   temp2                   ; Plus 4 clock cycles equals 0.2us
      brne  PV3                     ; Subtotal equals 2.45us
      ldi   temp,0b00110100         ; Load pass signal unaltered
      out   PORTB,temp              ; Output pass signal unaltered
      rjmp  PV1                     ; Return to test
PV4:
      sbic  $10,5                   ; Field Detect
      rjmp  ONE                     ; Go to PAL/SECAM Field One subroutine
      rjmp  TWO                     ; Go to PAL/SECAM field Two subroutine

;*******************************************************************************
;
; Field One subroutine for PAL/SECAM video signal input

ONE:
      nop                           ;
      ldi   temp,0b00001100         ; Load field one P-P half-line
      out   PORTB,temp               ; Output field one P-P half-line
      ldi   temp2,$C3               ; Load 29.25us ($C2=195; 195 x 0.15 = 29.25)
P11:
      dec   temp2                   ; Plus 3 clock cycles equals 0.15us
      brne  P11                     ; 2.35 + 29.25 + 0.15 = 31.75us
      ldi   temp1,18                ; Load VBI lines 6 thru 23, inclusive
P12:
      ldi   temp,0b00110100         ; Load pass signal unaltered
      out   PORTB,temp              ; Output pass signal unaltered
P13:
      sbic  $10,4                   ; Test for horizontal sync pulse
      rjmp  P13                     ; Return to test
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      ldi   temp,0b00100000        ; Load horizontal sync pulse
      out   PORTB,temp             ; Output horizontal sync pulse
      ldi   temp2,$1D              ; Load 4.35us ($1D=29; 29 x 0.15 = 4.35)
P14:
      dec   temp2                  ; Plus 7 clock cycles equals 0.35us
      brne  P14                    ; Subtotal equals 4.7us
      nop                          ;
      ldi   temp,0b00011100        ; Load breezeway and subcarrier
      out   PORTB,temp             ; Output breezeway and subcarrier
      ldi   temp2,$16              ; Load 3.3us ($16=22; 22 x 0.15 = 3.3)
P15:
      dec   temp2                  ; Plus 2 clock cycles equals 0.1us
      brne  P15                    ; Subtotal equals 3.4us
      ldi   temp,0b00001100        ; Load back porch remainder and P-P full line
      out   PORTB,temp             ; Output back porch remainder and P-P full line
      ldi   temp2,$D7              ; Load 53.75us ($D7=215; 215 x 0.25 = 53.75)
P16:
      nop                          ; Plus 5 clock cycles equals 0.25us
      nop                          ; Subtotal equals 54.0us
      dec   temp2                  ; Line total equals 62.1us
      brne  P16                    ; 1.65us front porch not included
      dec   temp1                  ; Countdown VBI lines
      brne  P12                    ; Finish VBI lines
      nop                          ;
      ldi   temp,0b00110100        ; Load pass signal unaltered
      out   PORTB,temp             ; Output pass signal unaltered
      reti                         ; Wait for next vertical pulse

;*************************************************************************************
;
; Field Two subroutine for PAL/SECAM video signal input

TWO:
      ldi   temp1,18               ; Load VBI lines 318 thru 335, inclusive
      nop                          ;
      nop                          ;
      ldi   temp2,$0F              ; Load 2.25us ($0F=15; 15 x 0.15 = 2.25)
P21:
      dec   temp2                  ; Plus 16 clock cycles equals 0.8us
      brne  P21                    ; 1.65 + 0.8 + 2.25 = 4.7us
      ldi   temp,0b00011100        ; Load breezeway and subcarrier
      out   PORTB,temp             ; Output breezeway and subcarrier
      ldi   temp2,$16              ; Load 3.3us ($16=22; 22 x 0.15 = 3.3)
P22:
      dec   temp2                  ; Plus 2 cycles equals 0.1us
      brne  P22                    ; Subtotal equals 3.4us
      ldi   temp,0b00001100        ; Load back porch remainder and P-P full line
      out   PORTB,temp             ; Output back porch remainder and P-P full line
      ldi   temp2,$D7              ; Load 53.75us ($D7=215; 215 x 0.25 = 53.75)
P23:
      nop                          ; Plus 5 clock cycles equals 0.25us
      nop                          ; Subtotal equals 54.0us
      dec   temp2                  ; Line total equals 62.1us
      brne  P23                    ;
      nop                          ;
      nop                          ;
      nop                          ;
P24:
      ldi   temp,0b00110100        ; Load pass signal unaltered
      out   PORTB,temp             ; Output pass signal unaltered
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P25:
      sbic  $10,4                ; Test for horizontal sync pulse
      rjmp  P25                  ; Return to test
      ldi   temp,0b00100000      ; Load horizontal sync pulse
      out   PORTB,temp           ; Output horizontal sync pulse
      ldi   temp2,$1D            ; Load 4.35us ($1D=29; 29 x 0.15 = 4.35)
P26:
      dec   temp2                ; Plus 7 clock cycles equals 0.35us
      brne  P26                  ; Subtotal equals 4.7us
      nop                        ;
      ldi   temp,0b00011100      ; Load breezeway and subcarrier
      out   PORTB,temp           ; Output breezeway and subcarrier
      ldi   temp2,$16            ; Load 3.3us ($16=22; 22 x 0.15 = 3.3)
P27:
      dec   temp2                ; Plus 2 clock cycles equals 0.1us
      brne  P27                  ; Subtotal equals 3.4us
      ldi   temp,0b00001100      ; Load back porch remainder and P-P full line
      out   PORTB,temp           ; Output back porch remainder and P-P full line
      ldi   temp2,$D7            ; Load 53.75us ($D7=215; 215 x 0.25 = 53.75)
P28:
      nop                        ; Plus 5 clock cycles equals 0.25us
      nop                        ; Subtotal equals 54.0us
      dec   temp2                ; Line total equals 62.1us
      brne  P28                  ; 1.65us front porch not included
      dec   temp1                ; Countdown VBI lines
      brne  P24                  ; Finish VBI lines
      nop                        ;
      ldi   temp,0b00110100      ; Load pass signal unaltered
      out   PORTB,temp           ; Output pass signal unaltered
      reti                       ; Wait for next vertical pulse
```