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;* MULTIPLE FORMAT VIDEO AGC/SYNC LOOP REGULATOR *  
;* Written by: J.L.K. Electronics *  
;* Date: November 1, 2008 *  
;* Version: J *  
;* Format: NTSC *  
;* Mode: Basic VBI Regulation of NTSC SDTV format *  
;* MCU: ATtiny2313/V *  
;* Clock Frequency: 20 MHz *  
;* Reference Generator: LM1881 *  
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; Program regulates the sync signal during the vertical Blanking Interval (VBI) of the NTSC SDTV format in the most basic form. The detection of the vertical sync pulse generates an interrupt in the main loop program. The program directs the microcontroller (MCU) to pass the remaining vertical pulses unaltered. The sync regulation begins with the post-equalizing pulse processing sub-routine, at the end of which the program directs the MCU to read the current field determined by the LM1881 reference generator. The current field subroutine (even or odd) is then selected and executed for the remainder of the VBI. Upon completion of the subroutine, the program allows the video signal to pass unaltered. The program returns from the interrupt to the main loop program until the next vertical sync pulse. It is of particular interest to note that the program may be allowed to continue throughout the entire field. This would encompass processing only the horizontal sync pulse and back porch of the horizontal blanking interval (HBI), allowing the front porch of the HBI and the active video to pass unaltered.

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.include "Tn2313def.inc"
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; Interrupt service vectors
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.org $0000  
    rjmp RESET                          ; Reset vector  
.org INT1addr  
    rjmp INTV1                          ; Int1 vector (external interrupt from pin PD3)
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; Declarations
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.def temp    =r16                      ; Output to Port B in binary  
.def temp1   =r17                      ; Pulse count in decimal  
.def temp2   =r18                      ; Time cycles in hex  
.def temp3   =r19                      ; Time cycle overflow in decimal
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; Reset vector just sets up interrupts and service routine and then loops forever
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RESET:
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    ldi temp,LOW(RAMEND)              ; Stack pointer  
    out SPL,temp                      ;  
  
    ldi temp,0b11111111              ; Port B - Outputs  
    out DDRB,temp                      ;  
    ldi temp,0b00000000              ; Port D - Inputs  
    out DDRD,temp                      ;
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    ldi    temp,0b00110100    ; Let all signals pass unaltered
    out    PORTB,temp        ;
    ldi    temp,0b11111111    ; Pull-ups on all inputs
    out    PORTD,temp        ;

; Set up interrupt INT1

    ldi    temp,0b10000000    ; Int1 selected
    out    GIMSK,temp        ;
    ldi    temp,0b00001000    ; Falling edge of Int1
    out    MCUCR,temp        ;

    sei                    ; Set global interrupt flag

LOOP:
    rjmp   LOOP                ;

;*****
;
; INT1 vector - passes vertical pulses unaltered - generates post-equalizing pulses
;               - determines field subroutine

INTV1:
    sbic   $10,4                ; Test for first serration completion
    rjmp   INTV1                ; Return to test
    ldi    temp3,5                ; Load vertical serration/pulse time overflow
V1:
    ldi    temp2,$D2            ; Load 31.5us ($D2=210; 210 x 0.15 = 31.5)
V2:
    dec    temp2                ;
    brne   V2                  ;
    dec    temp3                ;
    brne   V1                  ;
    ldi    temp1,6                ; Load six post-equalizing pulses
V3:
    sbic   $10,4                ; Test for post-equalizing pulse
    rjmp   V3                  ; Return to test
    ldi    temp,0b00100000        ; Load post-equalizing pulse
    out    PORTB,temp            ; Output post-equalizing pulse
    ldi    temp2,$0B            ; Load 1.65us ($0B=11; 11 x 0.15 = 1.65)
V4:
    dec    temp2                ; Plus 13 clock cycles equals 0.65us
    brne   V4                  ; Subtotal equals 2.3us
    dec    temp1                ;
    breq   V6                  ;
    nop                    ;
    nop                    ;
    nop                    ;
    nop                    ;
    nop                    ;
    ldi    temp,0b00001100        ; Load P-P interval
    out    PORTB,temp            ; Output P-P interval
    ldi    temp2,$C2            ; Load 29.1us ($C2=194; 194 x 0.15 = 29.1)
V5:
    dec    temp2                ; Plus 4 clock cycles equals 0.2us
    brne   V5                  ; Subtotal equals 29.3us
    ldi    temp,0b00110100        ; Load pass signal unaltered
    out    PORTB,temp            ; Output pass signal unaltered
    rjmp   V3                  ; Return to test
V6:

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        sbic  $10,5           ; Field detect
        rjmp  ODD           ; Go to Odd field subroutine
        rjmp  EVEN          ; Go to Even field subroutine

;*****
;
; Odd field subroutine for NTSC SDTV video signal input

ODD:
        nop                ;
        ldi   temp,0b00001100 ; Load odd field P-P half-line
        out  PORTB,temp     ; Output odd field half-line
        ldi   temp2,$C1     ; Load 28.95us ($C1=193; 193 x 0.15 = 28.95)
01:
        dec  temp2         ; Plus 3 clock cycles equals 0.15us
        brne O1           ; 2.3 + 28.95 + 0.15 = 31.4us
        ldi  temp1,11     ; Load VBI lines 10 thru 20, inclusive
02:
        ldi  temp,0b00110100 ; Load pass signal unaltered
        out  PORTB,temp     ; Output pass signal unaltered
03:
        sbic  $10,4         ; Test for horizontal sync pulse
        rjmp  O3           ; Return to test
        ldi  temp,0b00100000 ; Load horizontal sync pulse
        out  PORTB,temp     ; Output horizontal sync pulse
        ldi  temp2,$1D     ; Load 4.35us (1D=29; 29 x 0.15 = 4.35)
04:
        dec  temp2         ; Plus 7 clock cycles equals 0.35us
        brne O4           ; Subtotal equals 4.7us
        nop                ;
        ldi  temp,0b00011100 ; Load breezeway and colorburst
        out  PORTB,temp     ; Output breezeway and colorburst
        ldi  temp2,$16     ; Load 3.3us ($16=22; 22 x 0.15 = 3.3)
05:
        dec  temp2         ; Plus 2 clock cycles equals 0.1us
        brne O5           ; Subtotal equals 3.4us
        ldi  temp,0b00001100 ; Load back porch remainder and P-P full line
        out  PORTB,temp     ; Output back porch remainder and P-P full line
        ldi  temp2,$D6     ; Load 53.5us ($D6=214; 214 x 0.25 = 53.5)
06:
        nop                ; Plus 5 clock cycles equals 0.25us
        nop                ; Subtotal equals 53.75us
        dec  temp2         ; Line total equals 61.85us
        brne O6           ; 1.5us front porch not included
        dec  temp1         ; Countdown VBI lines
        brne O2           ; Finish VBI lines
        nop                ;
        ldi  temp,0b00110100 ; Load pass signal unaltered
        out  PORTB,temp     ; Output pass signal unaltered
        reti              ; Wait for next vertical pulse

;*****
;
; Even field subroutine for NTSC SDTV video signal input

EVEN:
        ldi  temp1,11     ; Load VBI lines 273 thru 283, inclusive
        nop                ;
        nop                ;
        ldi  temp2,$0F     ; Load 2.25us ($0F=15; 15 x 0.15 = 2.25)

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E1:
    dec    temp2                ; Plus 16 clock cycles equals 0.8us
    brne   E1                  ; 1.65 + 0.8 + 2.25 = 4.7us
    ldi    temp,0b00011100      ; Load breezeway and colorburst
    out    PORTB,temp           ; Output breezeway and colorburst
    ldi    temp2,$16            ; Load 3.3us ($16=22; 22 x 0.15 = 3.3)

E2:
    dec    temp2                ; Plus 2 clock cycles equals 0.1us
    brne   E2                  ; Subtotal equals 3.4us
    ldi    temp,0b00001100      ; Load back porch remainder and P-P full line
    out    PORTB,temp           ; Output back porch remainder and P-P full line
    ldi    temp2,$D6            ; Load 53.5us ($D6=214; 214 x 0.25 = 53.5)

E3:
    nop                                ; Plus 5 clock cycles equals 0.25us
    nop                                ; Subtotal equals 53.75us
    dec    temp2                ; Line totals equals 61.85us
    brne   E3                  ;
    nop                                ;
    nop                                ;
    nop                                ;

E4:
    ldi    temp,0b00110100      ; Load pass signal unaltered
    out    PORTB,temp           ; Output pass signal unaltered

E5:
    sbic   $10,4                ; Test for horizontal sync pulse
    rjmp   E5                  ; Return to test
    ldi    temp,0b00100000      ; Load horizontal sync pulse
    out    PORTB,temp           ; Output horizontal sync pulse
    ldi    temp2,$1D            ; Load 4.35us ($1D=29; 29 x 0.15 = 4.35)

E6:
    dec    temp2                ; Plus 7 clock cycles equals 0.35us
    brne   E6                  ; Subtotal equals 4.7us
    nop                                ;
    ldi    temp,0b00011100      ; Load breezeway and colorburst
    out    PORTB,temp           ; Output breezeway and colorburst
    ldi    temp2,$16            ; Load 3.3us ($16=22; 22 x 0.15 = 3.3)

E7:
    dec    temp2                ; Plus 2 clock cycles equals 0.1us
    brne   E7                  ; Subtotal equals 3.4us
    ldi    temp,0b00001100      ; Load back porch remainder and P-P full line
    out    PORTB,temp           ; Output back porch remainder and P-P full line
    ldi    temp2,$D6            ; Load 53.5us ($D6=214; 214 x 0.15 = 53.5)

E8:
    nop                                ; Plus 5 clock cycles equals 0.25us
    nop                                ; Subtotal equals 53.75us
    dec    temp2                ; Line total equals 61.85us
    brne   E8                  ; 1.5us front porch not included
    dec    temp1                ; Countdown VBI lines
    brne   E4                  ; Finish VBI lines
    nop                                ;
    ldi    temp,0b00110100      ; Load pass signal unaltered
    out    PORTB,temp           ; Output pass signal unaltered
    reti                                ; Wait for next vertical pulse

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